

40. (New) The system of Claim 39, wherein the field programmable gate array further comprises:

a second fixed logic processor embedded within the logic fabric; and

a second auxiliary processing interface that couples the second fixed logic processor to the first configured processor to perform the first fixed logic function.

41. (New) The system of Claim 39, wherein:

in the field programmable gate array a second portion of the logic fabric is configured as a second configured processor to perform a second fixed logic function; and

the field programmable gate array further comprises a second auxiliary processing interface that couples the second configured processor to perform the second fixed logic function to the fixed logic processor.

42. (New) The system of Claim 39, wherein:

in the field programmable gate array a second portion of the logic fabric is configured as a second configured processor to perform a second fixed logic function; and

the field programmable gate array further comprises addressing means for enabling the fixed logic processor to address the first configured processor to perform the first fixed logic function or the second configured processor to perform the second fixed logic function.

43. (New) The system of Claim 39, wherein:

in the field programmable gate array a second portion of the logic fabric is configured as a second configured processor to perform a second fixed logic function; and

the field programmable gate array further comprises:

a second fixed logic processor embedded within the logic fabric; and

91 a second auxiliary processing interface that couples the second fixed logic processor to the second configured processor to perform the second fixed logic function.

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